FIG.1

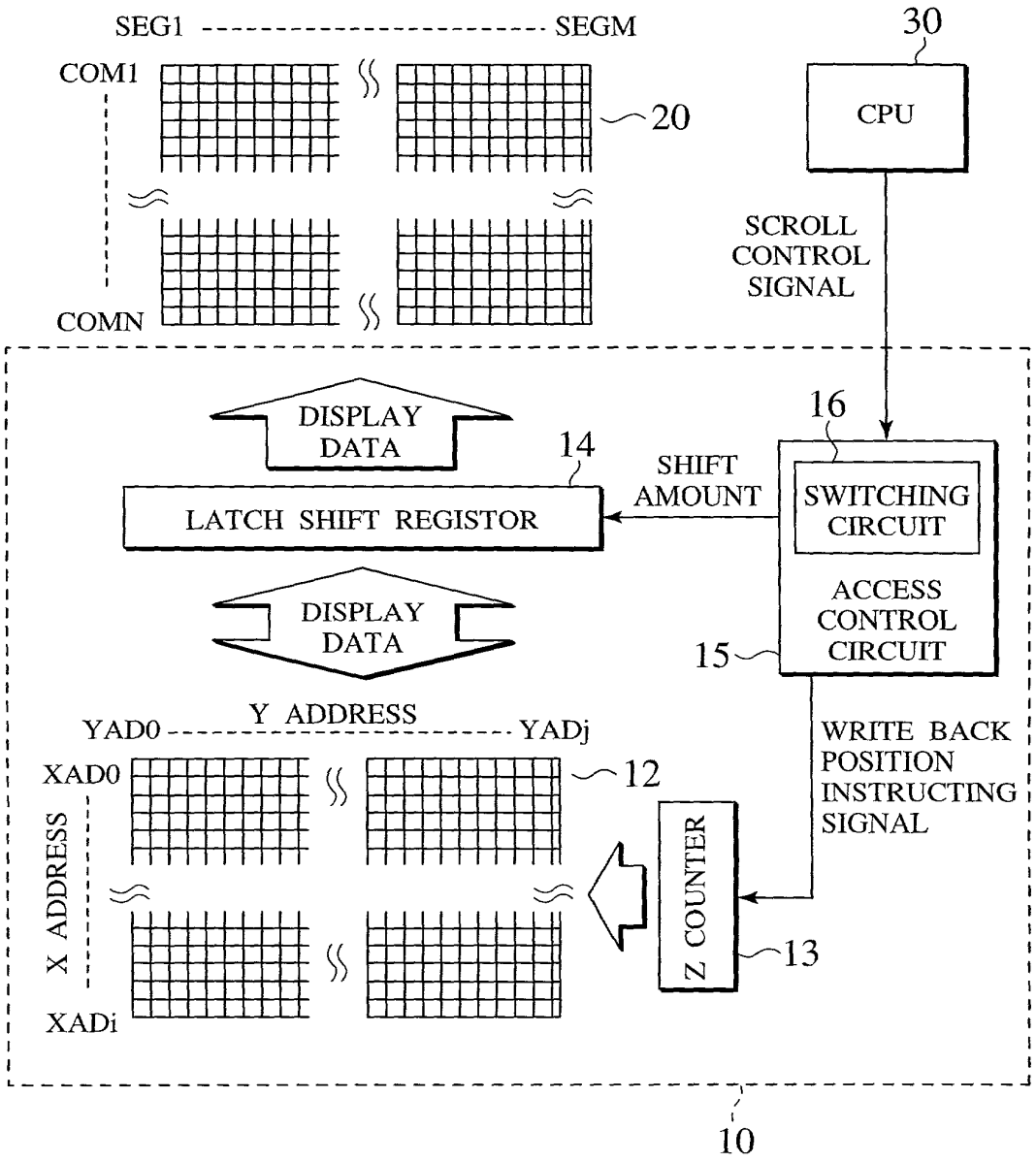

SEG1
SEGM
COM1
COMN
20
30
CPU
SCROLL CONTROL SIGNAL
16
DISPLAY DATA
14
SHIFT AMOUNT
SWITCHING CIRCUIT
LATCH SHIFT REGISTOR
DISPLAY DATA
ACCESS CONTROL CIRCUIT
15
Y ADDRESS
YAD0
YADj
XAD0
12
X ADDRESS
WRITE BACK POSITION INSTRUCTING SIGNAL
Z COUNTER
13
XADi
10

FIG.2

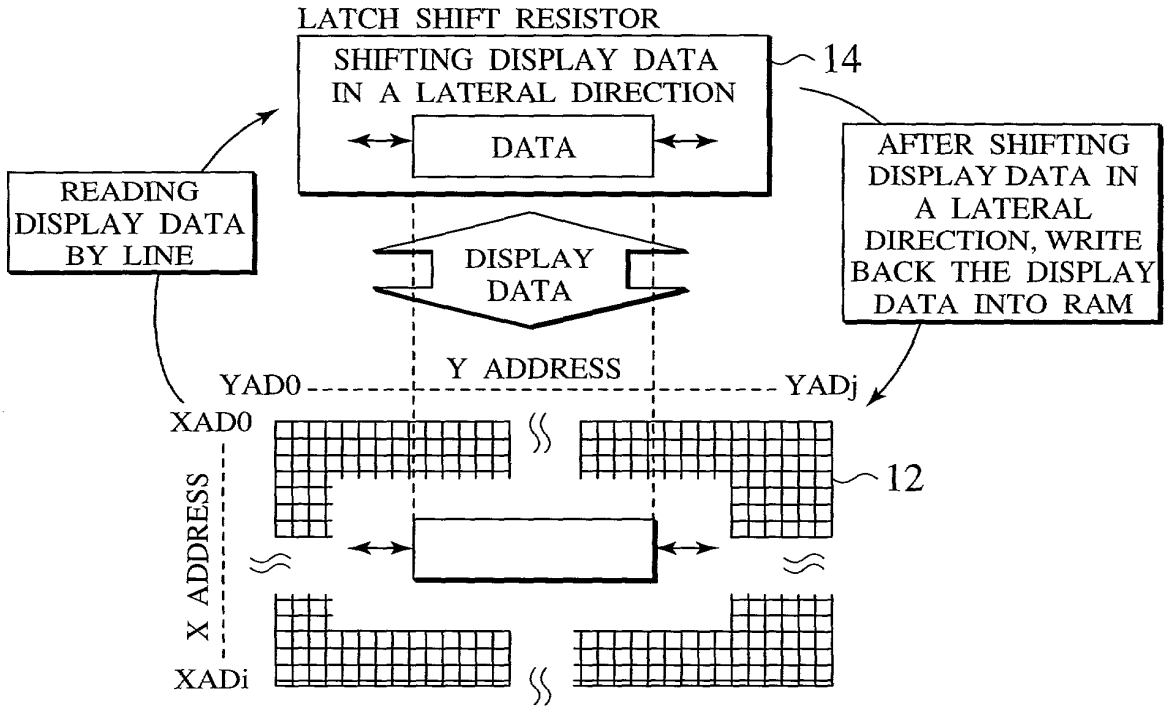


FIG.3A

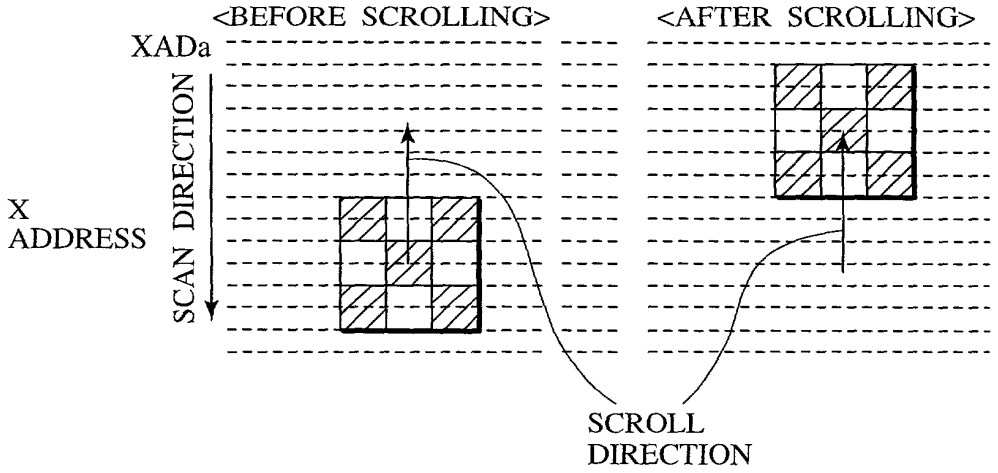


FIG.3B

FIG.4

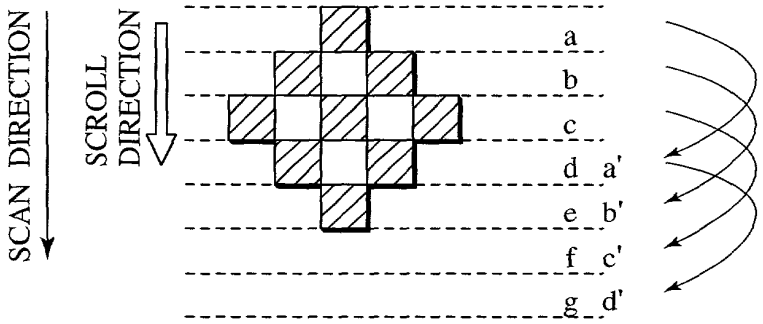


FIG.5A

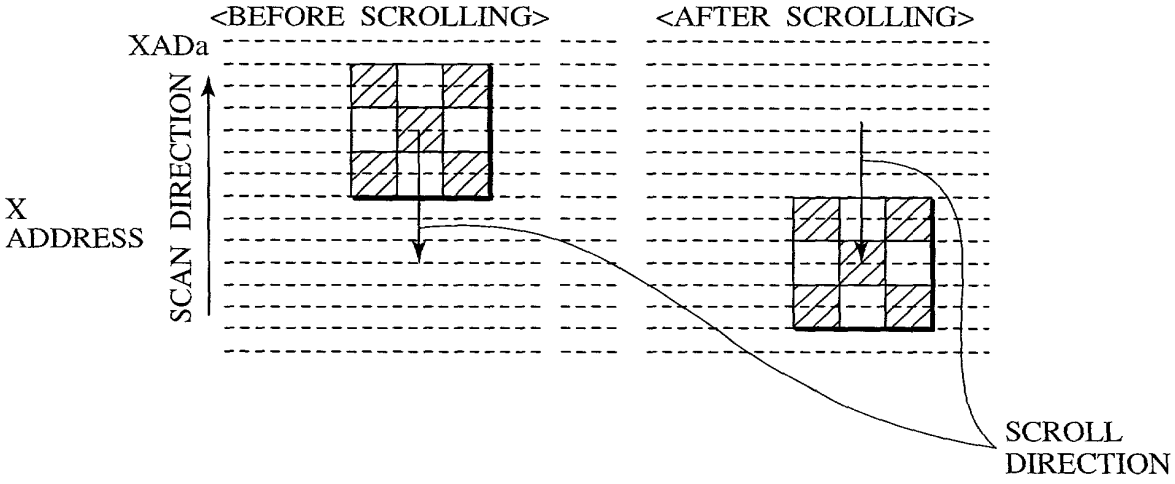


FIG.5B

FIG.6

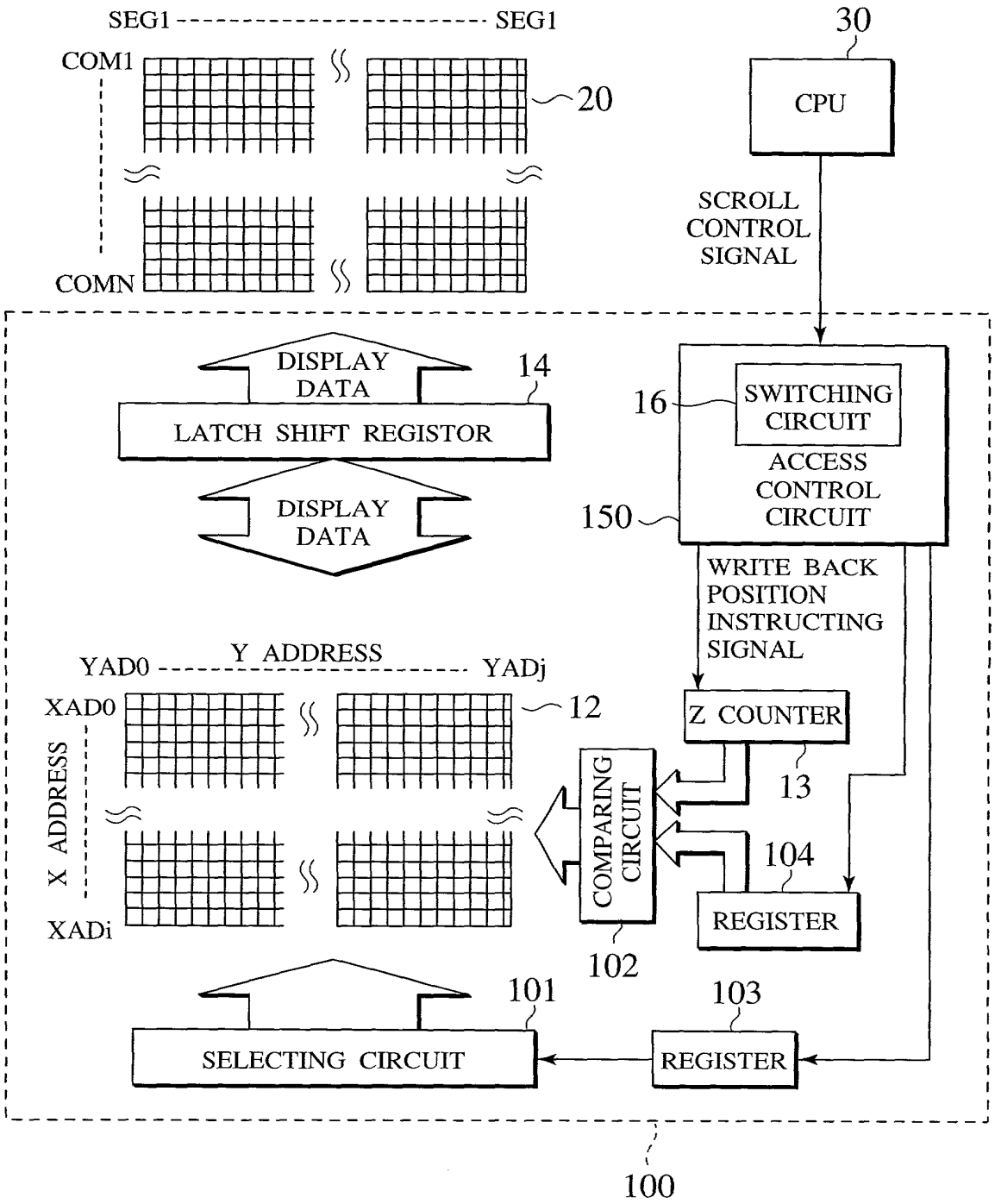

SEG1
SEG1
COM1
COMN
20
30
CPU
SCROLL CONTROL SIGNAL
DISPLAY DATA
14
LATCH SHIFT REGISTOR
DISPLAY DATA
16
SWITCHING CIRCUIT
ACCESS CONTROL CIRCUIT
150
WRITE BACK POSITION INSTRUCTING SIGNAL
Y ADDRESS
YAD0
YADj
XAD0
XADi
X ADDRESS
12
Z COUNTER
13
COMPARING CIRCUIT
104
REGISTER
102
101
SELECTING CIRCUIT
103
REGISTER
100

FIG.7

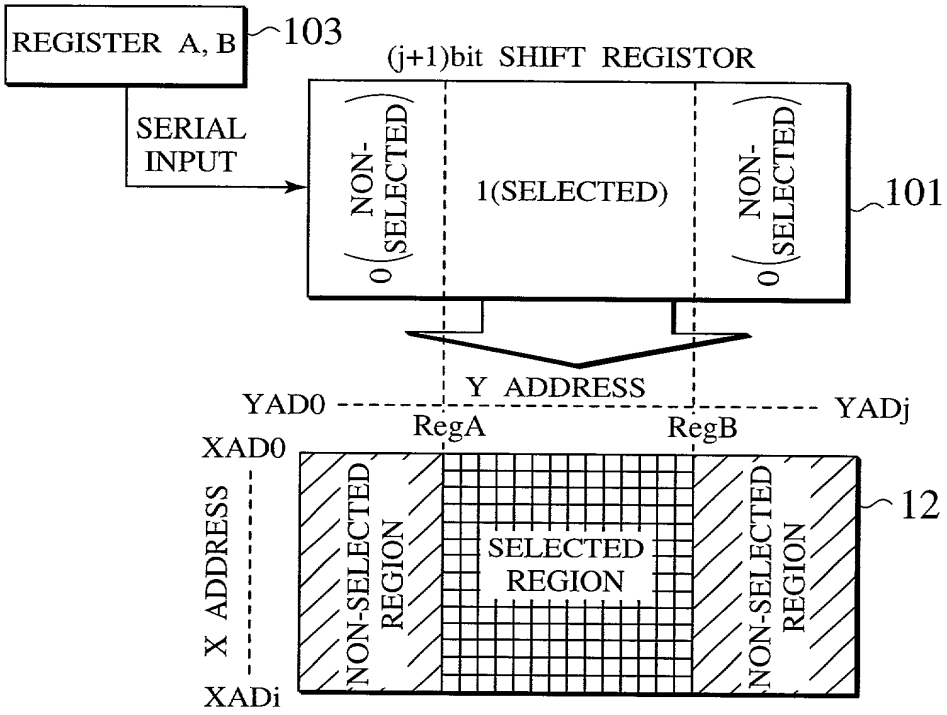
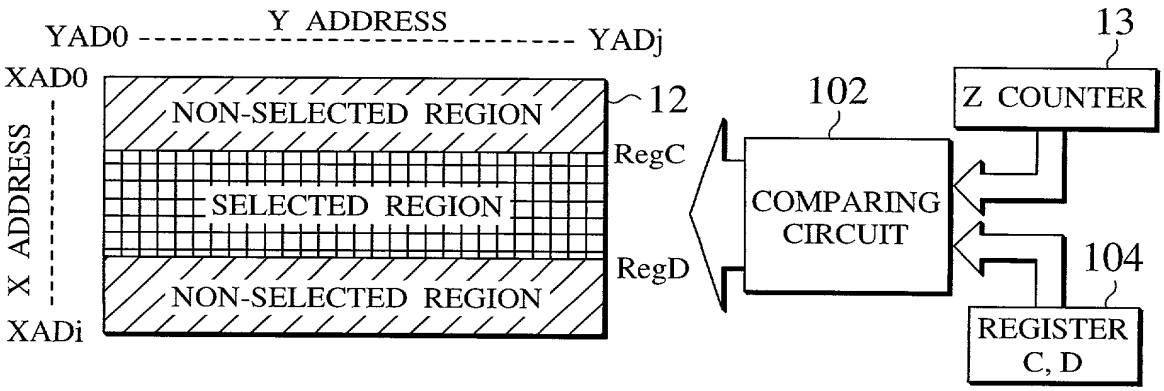

REGISTER A, B
103
(j+1)bit SHIFT REGISTOR
SERIAL INPUT
0 (NON-SELECTED)
1(SELECTED)
0 (NON-SELECTED)
101
Y ADDRESS
YAD0
YADj
RegA
RegB
XAD0
X ADDRESS
XADi
NON-SELECTED REGION
SELECTED REGION
NON-SELECTED REGION
12

FIG.8


YAD0
Y ADDRESS
YADj
XAD0
X ADDRESS
XADi
NON-SELECTED REGION
12
RegC
SELECTED REGION
RegD
NON-SELECTED REGION
102
COMPARING CIRCUIT
13
Z COUNTER
104
REGISTER C, D